```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 20
description:
top level BOM
----------------------------
revision 3.644
date: 1995/04/28 06:31:37;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

try and avoid collisions in top level
----------------------------
revision 3.643
date: 1995/04/28 05:39:09;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 3.642
date: 1995/04/27 21:12:14;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

gt/pimlib.pl:  Move tau1[ab] drivers from the left side to the right side so
  that they will be near clumped loads to fix dcload violation.
----------------------------
revision 3.641
date: 1995/04/27 01:20:41;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc
      verify.html

change wording for address-test switch for hermes model
----------------------------
revision 3.640
date: 1995/04/27 00:20:25;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
```

```
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
iq/iq.V:  Remove dead predGoQ5 wire decl.
euterpe.status:  Over the last few BOMs:
  fullswing cb4 input to gtsnake (UUetaUTR11[2]) was fixed to halfswing,
  broken SMUX instructions were made reserved a few BOMs ago,
  ITag data out was reduced from hr to flop in choke corridor,
  ICC bus into ITag data in reg was made psuedo-diff in choke corridor.
----------------------------
revision 3.639
date: 1995/04/26 18:28:00;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

update placement.
----------------------------
revision 3.638
date: 1995/04/26 08:39:34;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 3.637
date: 1995/04/25 23:17:42;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.
```

```
atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy. *not complete*

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.

placement updates to follow.
CVS: ----------------------------------------------------------------------
CVS: Enter Log.  Lines beginning with `CVS: ' are removed automatically
CVS:
CVS: Committing in
CVS:
CVS: Modified Files:
CVS:  euterpe.V
CVS: ----------------------------------------------------------------------
----------------------------
revision 3.636
date: 1995/04/25 16:06:19;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/include

New macros added for the global access field in CO6.
----------------------------
revision 3.635
date: 1995/04/25 06:51:28;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 3.634
date: 1995/04/25 02:50:36;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

euterpe.status gt/gtsnake.V gt/pimlib.pl:
  Convert full- to half-swing load on busy toplevel net UUetaUTR11.
----------------------------
revision 3.633
date: 1995/04/25 01:48:48;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

gt/gt.V gt/genpim.pl gt/pimlib.pl:  Add dedicated tau for 107uA GTLB.
  Move tau0a & tau0b drivers from genpim.pl to pimlib.pl's miscstuff subroutine
```

```
  and get on proper row.
gt/genptab.pl:  dickson fix csyn error; geert removed UgvaR8R9[ab] power set.
----------------------------
revision 3.632
date: 1995/04/24 17:15:39;  author: vo;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cg

added cgclockbias.sp to list of things to make
----------------------------
revision 3.631
date: 1995/04/24 11:13:11;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 3.630
date: 1995/04/24 03:25:57;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mst
```

```
solve dc load problems
----------------------------
revision 3.629
date: 1995/04/23 03:58:14;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

solve dc load problems
----------------------------
revision 3.628
date: 1995/04/22 23:35:33;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

fix dc load problem
----------------------------
revision 3.627
date: 1995/04/22 23:33:22;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

fix dc load problem
----------------------------
revision 3.626
date: 1995/04/22 17:24:22;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

solve dc load problem
----------------------------
revision 3.625
date: 1995/04/22 17:17:01;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

solve dc load problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/BOM,v
Working file: doc/BOM
head: 22.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 1
description:
BOM for doc
----------------------------
revision 19.3
date: 1995/04/27 01:20:20;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc
      verify.html

change wording for address-test switch for hermes model
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/verify.html,v
Working file: doc/verify.html
head: 18.20
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 18.14
date: 1995/04/27 01:19:13;  author: doi;  state: Exp;  lines: +7 -7
change wording for address-test switch for hermes model
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 1
description:
----------------------------
revision 4.103
date: 1995/04/25 16:06:05;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/include

New macros added for the global access field in CO6.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/BOM,v
Working file: verify/include/BOM
head: 36.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 28.0
date: 1995/04/25 16:05:54;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/include

New macros added for the global access field in CO6.
----------------------------
revision 27.1
date: 1995/04/25 16:05:47;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/include/cerberus.h,v
Working file: verify/include/cerberus.h
head: 10.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 1
```

```
description:
----------------------------
revision 10.16
date: 1995/04/24 22:44:35;  author: jeffm;  state: Exp;  lines: +23 -1
New macros added for the global access field in CO6.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 3
description:
----------------------------
revision 1.147
date: 1995/04/27 23:12:42;  author: jeffm;  state: Exp;  lines: +2 -2
Make sure all tags uniquely addressable, and accessable independent
of cache size.
----------------------------
revision 1.146
date: 1995/04/26 00:39:15;  author: jeffm;  state: Exp;  lines: +2 -2
Check nb load/use dependency checking for ggfmul8 - expected to fail on HW.
----------------------------
revision 1.145
date: 1995/04/24 22:17:11;  author: jeffm;  state: Exp;  lines: +2 -2
Basic test of the functions of the global access field in cerberus octlet 6.
Does not pass terp - probable terp bug.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/cerb_perf.S,v
Working file: verify/perf/cerb_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 2
description:
----------------------------
revision 1.2
date: 1995/04/27 21:34:05;  author: claseman;  state: Exp;  lines: +2 -2
add null to register 61 not 60
----------------------------
revision 1.1
date: 1995/04/26 22:17:48;  author: claseman;  state: Exp;
initial revision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/dram_perf.S,v
Working file: verify/perf/dram_perf.S
head: 1.8
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
----------------------------
revision 1.2
date: 1995/04/27 21:34:07;  author: claseman;  state: Exp;  lines: +2 -2
add null to register 61 not 60
----------------------------
revision 1.1
date: 1995/04/26 22:17:46;  author: claseman;  state: Exp;
initial revision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/hermes_perf.S,v
Working file: verify/perf/hermes_perf.S
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 2
description:
----------------------------
revision 1.3
date: 1995/04/27 21:34:08;  author: claseman;  state: Exp;  lines: +2 -2
add null to register 61 not 60
----------------------------
revision 1.2
date: 1995/04/26 22:17:43;  author: claseman;  state: Exp;  lines: +83 -27
initial revision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/rom_perf.S,v
Working file: verify/perf/rom_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 2
description:
----------------------------
revision 1.2
date: 1995/04/27 21:34:10;  author: claseman;  state: Exp;  lines: +2 -2
add null to register 61 not 60
----------------------------
revision 1.1
date: 1995/04/26 22:17:49;  author: claseman;  state: Exp;
initial revision
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/NOTES,v
Working file: verify/standalone/hc/NOTES
head: 1.28
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 1.25
date: 1995/04/27 15:40:10;  author: brian;  state: Exp;  lines: +32 -0
Added some NOTES. Fiddled with gauntlet test.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/clkregress.pl,v
Working file: verify/standalone/hc/clkregress.pl
head: 7.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 7.12
date: 1995/04/27 15:40:12;  author: brian;  state: Exp;  lines: +2 -2
Added some NOTES. Fiddled with gauntlet test.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/gauntlet.vec,v
Working file: verify/standalone/hc/gauntlet.vec
head: 8.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 8.2
date: 1995/04/27 15:40:13;  author: brian;  state: Exp;  lines: +6 -12
Added some NOTES. Fiddled with gauntlet test.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/nbhc_drive.V,v
Working file: verify/standalone/hc/nbhc_drive.V
head: 1.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;    selected revisions: 1
description:
----------------------------
revision 1.48
date: 1995/04/27 15:40:15;  author: brian;  state: Exp;  lines: +3 -3
Added some NOTES. Fiddled with gauntlet test.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/Attic/startup.pl,v
Working file: verify/standalone/hc/startup.pl
head: 8.3
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 8.3
date: 1995/04/27 15:40:17;  author: brian;  state: Exp;  lines: +2 -2
Added some NOTES. Fiddled with gauntlet test.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/NOTES,v
Working file: verify/standalone/nb/NOTES
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 1.15
date: 1995/04/27 15:41:20;  author: brian;  state: Exp;  lines: +37 -0
Reviewed the way the driver measures load timing. Made a minor change
described in NOTES.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/nb/nb_drive.V,v
Working file: verify/standalone/nb/nb_drive.V
head: 1.40
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 40;    selected revisions: 1
description:
----------------------------
revision 1.40
date: 1995/04/27 15:41:24;  author: brian;  state: Exp;  lines: +19 -11
Reviewed the way the driver measures load timing. Made a minor change
described in NOTES.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/ruptpintest.S,v
Working file: verify/standalone/uu/ruptpintest.S
head: 8.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 2
description:
----------------------------
revision 8.3
date: 1995/04/27 22:23:38;  author: jeffm;  state: Exp;  lines: +16 -30
Fixed a couple more bugs in the test.
```

```
----------------------------
revision 8.2
date: 1995/04/27 20:00:58;  author: jeffm;  state: Exp;  lines: +4 -2
Fixed mask used to enable for rupts - were not enabling the right bit.
Wiggle the big later - to allow for time to come out of reset and
to do initialization. NOTE: The test will now run for about
2.8 million simtics.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/ruptpintest.sen,v
Working file: verify/standalone/uu/ruptpintest.sen
head: 8.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 8.2
date: 1995/04/27 20:01:01;  author: jeffm;  state: Exp;  lines: +21 -21
Fixed mask used to enable for rupts - were not enabling the right bit.
Wiggle the big later - to allow for time to come out of reset and
to do initialization. NOTE: The test will now run for about
2.8 million simtics.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/el/apd2res1.c,v
Working file: verify/tools/el/apd2res1.c
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 1
description:
initial checkin
----------------------------
revision 1.63
date: 1995/04/24 17:30:17;  author: veena;  state: Exp;  lines: +4 -4
Register r32 was used as src1 pair and r33 for src2 which was incorrect.
replaced r32 with original register r12.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 3
description:
----------------------------
revision 1.147
date: 1995/04/27 23:12:42;  author: jeffm;  state: Exp;  lines: +2 -2
Make sure all tags uniquely addressable, and accessable independent
```

```
of cache size.
----------------------------
revision 1.146
date: 1995/04/26 00:39:15;  author: jeffm;  state: Exp;  lines: +2 -2
Check nb load/use dependency checking for ggfmul8 - expected to fail on HW.
----------------------------
revision 1.145
date: 1995/04/24 22:17:11;  author: jeffm;  state: Exp;  lines: +2 -2
Basic test of the functions of the global access field in cerberus octlet 6.
Does not pass terp - probable terp bug.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/cachesynchnasty2.S,v
Working file: verify/toplevel/cachesynchnasty2.S
head: 35.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 3
description:
----------------------------
revision 35.9
date: 1995/04/27 20:24:56;  author: jeffm;  state: Exp;  lines: +2 -2
Had not widened out the interrupt timing enough.
----------------------------
revision 35.8
date: 1995/04/26 18:23:07;  author: jeffm;  state: Exp;  lines: +17 -4
Fixed missing delay between store and load to different offsets of the
event register.

Turn off timer rupts before calling mpass.
----------------------------
revision 35.7
date: 1995/04/25 23:57:17;  author: jeffm;  state: Exp;  lines: +2 -2
Put more delay between rupts.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/frz_debug.sig,v
Working file: verify/toplevel/frz_debug.sig
head: 35.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 2
description:
----------------------------
revision 35.2
date: 1995/04/26 22:24:36;  author: jeffm;  state: Exp;  lines: +3 -2
Added signal anyLtXcR13.
----------------------------
revision 35.1
date: 1995/04/26 22:16:55;  author: jeffm;  state: Exp;
Split up prblm_debug.sig into prblm_debug.sig, frz_debug.sig, and ife_debug.sig.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/ife_debug.sig,v
Working file: verify/toplevel/ife_debug.sig
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/26 22:16:58;  author: jeffm;  state: Exp;
Split up prblm_debug.sig into prblm_debug.sig, frz_debug.sig, and ife_debug.sig.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ltlbga.S,v
Working file: verify/toplevel/ltlbga.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 35.2
date: 1995/04/25 16:47:17;  author: jeffm;  state: Exp;  lines: +25 -21
Fixed numerous bugs. Passes terp.
----------------------------
revision 35.1
date: 1995/04/24 22:17:08;  author: jeffm;  state: Exp;
Basic test of the functions of the global access field in cerberus octlet 6.
Does not pass terp - probable terp bug.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ltlbtran.S,v
Working file: verify/toplevel/ltlbtran.S
head: 33.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 33.3
date: 1995/04/26 18:58:47;  author: jeffm;  state: Exp;  lines: +2 -2
Uninitialized gtlb entry caused test to go to X.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/nbusemul.S,v
Working file: verify/toplevel/nbusemul.S
head: 35.3
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 3;     selected revisions: 3
description:
----------------------------
revision 35.3
date: 1995/04/26 23:42:05;  author: jeffm;  state: Exp;  lines: +185 -12
Added 6 more test cases - to test nb load/use w/o involving
nb anti-use. This test should run on the HW - the design hole
mentioned in euterpe.status is not exploitable, because the nb-anti use
protection covers the whole register pair, preventing the split register
write while the nb op is outstanding.
----------------------------
revision 35.2
date: 1995/04/26 16:10:54;  author: jeffm;  state: Exp;  lines: +9 -10
Improved data patterns - making the contents of the A,B, and C registers
unique.
----------------------------
revision 35.1
date: 1995/04/26 00:39:11;  author: jeffm;  state: Exp;
Check nb load/use dependency checking for ggfmul8 - expected to fail on HW.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/prblm_debug.sig,v
Working file: verify/toplevel/prblm_debug.sig
head: 33.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 2
description:
----------------------------
revision 33.6
date: 1995/04/25 18:39:25;  author: jeffm;  state: Exp;  lines: +6 -3
Signals for mws.
----------------------------
revision 33.5
date: 1995/04/25 00:14:38;  author: jeffm;  state: Exp;  lines: +10 -2
Added signals for exception lock/unlock.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/tagaccess.S,v
Working file: verify/toplevel/tagaccess.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/04/27 23:12:45;  author: jeffm;  state: Exp;
Make sure all tags uniquely addressable, and accessable independent
of cache size.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/wbck_debug.sig,v
```

```
Working file: verify/toplevel/wbck_debug.sig
head: 33.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 33.5
date: 1995/04/24 23:53:53;  author: jeffm;  state: Exp;  lines: +12 -1
Added more sigs.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 18
description:
top level verilog BOM
----------------------------
revision 3.516
date: 1995/04/28 06:31:21;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

try and avoid collisions in top level
----------------------------
revision 3.515
date: 1995/04/28 05:38:52;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 3.514
date: 1995/04/27 21:11:59;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

gt/pimlib.pl:  Move tau1[ab] drivers from the left side to the right side so
  that they will be near clumped loads to fix dcload violation.
```

```
----------------------------
revision 3.513
date: 1995/04/27 00:20:02;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
iq/iq.V:  Remove dead predGoQ5 wire decl.
euterpe.status:  Over the last few BOMs:
  fullswing cb4 input to gtsnake (UUetaUTR11[2]) was fixed to halfswing,
  broken SMUX instructions were made reserved a few BOMs ago,
  ITag data out was reduced from hr to flop in choke corridor,
  ICC bus into ITag data in reg was made psuedo-diff in choke corridor.
----------------------------
revision 3.512
date: 1995/04/26 18:27:40;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

update placement.
----------------------------
revision 3.511
date: 1995/04/26 08:39:17;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 3.510
date: 1995/04/25 23:17:22;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
```

```
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy. *not complete*

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.

placement updates to follow.
CVS: ----------------------------------------------------------------------
CVS: Enter Log.  Lines beginning with `CVS: ' are removed automatically
CVS:
CVS: Committing in
CVS:
CVS: Modified Files:
CVS:  euterpe.V
CVS: ----------------------------------------------------------------------
----------------------------
revision 3.509
date: 1995/04/25 06:51:09;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 3.508
date: 1995/04/25 02:50:18;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

euterpe.status gt/gtsnake.V gt/pimlib.pl:
  Convert full- to half-swing load on busy toplevel net UUetaUTR11.
----------------------------
revision 3.507
date: 1995/04/25 01:48:27;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

gt/gt.V gt/genpim.pl gt/pimlib.pl:  Add dedicated tau for 107uA GTLB.
```

```
  Move tau0a & tau0b drivers from genpim.pl to pimlib.pl's miscstuff subroutine
  and get on proper row.
gt/genptab.pl:  dickson fix csyn error; geert removed UgvaR8R9[ab] power set.
----------------------------
revision 3.506
date: 1995/04/24 17:15:18;  author: vo;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cg

added cgclockbias.sp to list of things to make
----------------------------
revision 3.505
date: 1995/04/24 11:12:52;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 3.504
date: 1995/04/24 03:25:42;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mst
```

. . .

```
solve dc load problems
----------------------------
revision 3.503
date: 1995/04/23 03:58:00;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

solve dc load problems
----------------------------
revision 3.502
date: 1995/04/22 23:35:20;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

fix dc load problem
----------------------------
revision 3.501
date: 1995/04/22 23:33:08;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

fix dc load problem
----------------------------
revision 3.500
date: 1995/04/22 17:24:03;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

solve dc load problem
----------------------------
revision 3.499
date: 1995/04/22 17:16:38;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

solve dc load problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 24
description:
----------------------------
revision 292.1
date: 1995/04/28 06:31:06;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

try and avoid collisions in top level
----------------------------
revision 292.0
date: 1995/04/28 05:38:32;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list
```

```
Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 291.2
date: 1995/04/28 05:38:19;  author: tbr;  state: Exp;  lines: +33 -33
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 291.1
date: 1995/04/27 21:11:44;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

gt/pimlib.pl:  Move tau1[ab] drivers from the left side to the right side so
  that they will be near clumped loads to fix dcload violation.
----------------------------
revision 291.0
date: 1995/04/27 00:19:39;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uuprblmr7.Vegn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
iq/iq.V:  Remove dead predGoQ5 wire decl.
euterpe.status:  Over the last few BOMs:
  fullswing cb4 input to gtsnake (UUetaUTR11[2]) was fixed to halfswing,
  broken SMUX instructions were made reserved a few BOMs ago,
  ITag data out was reduced from hr to flop in choke corridor,
  ICC bus into ITag data in reg was made psuedo-diff in choke corridor.
----------------------------
revision 290.2
date: 1995/04/27 00:19:22;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 290.1
date: 1995/04/26 18:27:21;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

update placement.
----------------------------
revision 290.0
date: 1995/04/26 08:38:59;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
```

```
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 289.1
date: 1995/04/26 08:38:46;  author: mws;  state: Exp;  lines: +10 -10
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 289.0
date: 1995/04/25 23:17:00;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy. *not complete*

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.

placement updates to follow.
CVS: ----------------------------------------------------------------------
CVS: Enter Log.  Lines beginning with `CVS: ' are removed automatically
CVS:
CVS: Committing in
CVS:
```

```
CVS: Modified Files:
CVS:  euterpe.V
CVS: ----------------------------------------------------------------------
----------------------------
revision 288.1
date: 1995/04/25 23:16:44;  author: woody;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 288.0
date: 1995/04/25 06:50:49;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 287.4
date: 1995/04/25 06:50:34;  author: tbr;  state: Exp;  lines: +23 -23
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 287.3
date: 1995/04/25 02:50:01;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

euterpe.status gt/gtsnake.V gt/pimlib.pl:
  Convert full- to half-swing load on busy toplevel net UUetaUTR11.
----------------------------
revision 287.2
date: 1995/04/25 01:48:08;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

gt/gt.V gt/genpim.pl gt/pimlib.pl:  Add dedicated tau for 107uA GTLB.
  Move tau0a & tau0b drivers from genpim.pl to pimlib.pl's miscstuff subroutine
  and get on proper row.
gt/genptab.pl:  dickson fix csyn error; geert removed UgvaR8R9[ab] power set.
----------------------------
revision 287.1
date: 1995/04/24 17:14:56;  author: vo;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cg

added cgclockbias.sp to list of things to make
----------------------------
revision 287.0
date: 1995/04/24 11:12:31;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.
```

```
euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 286.8
date: 1995/04/24 11:12:17;  author: mws;  state: Exp;  lines: +14 -14
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 286.7
date: 1995/04/24 03:25:28;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mst

solve dc load problems
----------------------------
revision 286.6
date: 1995/04/23 03:57:46;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

solve dc load problems
----------------------------
revision 286.5
date: 1995/04/22 23:35:07;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

fix dc load problem
----------------------------
```

. . .

```
revision 286.4
date: 1995/04/22 23:32:54;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

fix dc load problem
----------------------------
revision 286.3
date: 1995/04/22 17:23:44;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

solve dc load problem
----------------------------
revision 286.2
date: 1995/04/22 17:16:19;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

solve dc load problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255;   selected revisions: 2
description:
----------------------------
revision 1.238
date: 1995/04/26 06:30:46;  author: chip;  state: Exp;  lines: +2 -8
Changed chip exclude lits

Geert
----------------------------
revision 1.237
date: 1995/04/24 18:46:34;  author: lisar;  state: Exp;  lines: +4 -4
Fixed compv analyzes
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 3
description:
----------------------------
revision 40.71
date: 1995/04/27 22:42:31;  author: chip;  state: Exp;  lines: +2 -2
D Fixed a spacing  ... just cosmetic

Geert
----------------------------
revision 40.70
```

. . .

```
date: 1995/04/27 22:20:44;  author: chip;  state: Exp;  lines: +4 -4
Got rid of the -p4 from uu-local.obs

Geert
----------------------------
revision 40.69
date: 1995/04/25 01:11:09;  author: chip;  state: Exp;  lines: +4 -3
Changed the order of the -ter.pim make
from the base.pim make for the first pass.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.vo,v
Working file: verilog/bsrc/Makefile.vo
head: 27.45
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 45;    selected revisions: 1
description:
----------------------------
revision 27.30
date: 1995/04/24 19:24:58;  author: vo;  state: Exp;  lines: +2 -1
changed to unconditionally remove usefakedkmap directive .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;   selected revisions: 6
description:
----------------------------
revision 6.411
date: 1995/04/26 08:25:01;  author: mws;  state: Exp;  lines: +5 -4
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
----------------------------
revision 6.410
date: 1995/04/25 23:06:39;  author: woody;  state: Exp;  lines: +5 -2
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
```

```
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy.

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.
----------------------------
revision 6.409
date: 1995/04/25 08:05:46;  author: mws;  state: Exp;  lines: +20 -18
Correct GTtau stage suffix.
----------------------------
revision 6.408
date: 1995/04/25 06:43:10;  author: tbr;  state: Exp;  lines: +4 -3
added GTtauUW connection for new fannout buffer
----------------------------
revision 6.407
date: 1995/04/24 18:43:11;  author: dickson;  state: Exp;  lines: +1 -2
removed c01_1 at top level
----------------------------
revision 6.406
date: 1995/04/24 11:01:43;  author: mws;  state: Exp;  lines: +57 -33
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
==============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v
Working file: verilog/bsrc/euterpe.status
head: 24.83
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 83;    selected revisions: 5
description:
----------------------------
revision 24.64
date: 1995/04/27 00:10:48;  author: mws;  state: Exp;  lines: +8 -15
Over the last few BOMs:
  fullswing cb4 input to gtsnake (UUetaUTR11[2]) was fixed to halfswing,
  broken SMUX instructions were made reserved a few BOMs ago,
```

```
  ITag data out was reduced from hr to flop in choke corridor,
  ICC bus into ITag data in reg was made psuedo-diff in choke corridor.
----------------------------
revision 24.63
date: 1995/04/26 08:30:04;  author: mws;  state: Exp;  lines: +26 -32
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 24.62
date: 1995/04/25 03:32:41;  author: mws;  state: Exp;  lines: +10 -1
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 24.61
date: 1995/04/25 03:01:54;  author: mws;  state: Exp;  lines: +23 -2
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status gt/gtsnake.V gt/pimlib.pl:
  Convert full- to half-swing load on busy toplevel net UUetaUTR11.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
----------------------------
revision 24.60
date: 1995/04/24 11:02:47;  author: mws;  state: Exp;  lines: +29 -22
euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/.checkoutrc,v
Working file: verilog/bsrc/at/.checkoutrc
head: 4.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/04/23 05:44:16;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v
Working file: verilog/bsrc/at/BOM
head: 93.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 184;   selected revisions: 10
description:
releasebom adding BOM
----------------------------
revision 75.0
date: 1995/04/28 05:25:19;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 74.1
date: 1995/04/28 05:25:12;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 74.0
date: 1995/04/26 18:27:01;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/at

update placement.
----------------------------
revision 73.1
date: 1995/04/26 18:26:52;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 73.0
```

```
date: 1995/04/25 23:09:32;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy. *not complete*

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.

placement updates to follow.
CVS: ----------------------------------------------------------------------
CVS: Enter Log.  Lines beginning with `CVS: ' are removed automatically
CVS:
CVS: Committing in
CVS:
CVS: Modified Files:
CVS:  euterpe.V
CVS: ----------------------------------------------------------------------
----------------------------
revision 72.1
date: 1995/04/25 23:09:25;  author: woody;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 72.0
date: 1995/04/25 06:13:52;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 71.1
date: 1995/04/25 06:13:45;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 71.0
```

```
date: 1995/04/22 17:15:59;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/at

solve dc load problem
----------------------------
revision 70.1
date: 1995/04/22 17:15:52;  author: dickson;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.V,v
Working file: verilog/bsrc/at/at.V
head: 1.66
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 66;    selected revisions: 1
description:
----------------------------
revision 1.52
date: 1995/04/25 23:07:08;  author: woody;  state: Exp;  lines: +16 -6
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy.

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.pim,v
Working file: verilog/bsrc/at/at.pim
head: 51.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 3
description:
----------------------------
revision 51.13
date: 1995/04/26 18:26:12;  author: woody;  state: Exp;  lines: +9 -1
update placement.
```

```
----------------------------
revision 51.12
date: 1995/04/25 23:07:11;  author: woody;  state: Exp;  lines: +1 -1
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy.

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.
----------------------------
revision 51.11
date: 1995/04/22 17:15:01;  author: dickson;  state: Exp;  lines: +1362 -1363
solve dc load problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.power.tab.top,v
Working file: verilog/bsrc/at/at.power.tab.top
head: 28.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 28.8
date: 1995/04/28 04:48:08;  author: tbr;  state: Exp;  lines: +993 -955
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atpadcd.Veqn,v
Working file: verilog/bsrc/at/atpadcd.Veqn
head: 1.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 1
description:
----------------------------
revision 1.23
date: 1995/04/25 23:07:14;  author: woody;  state: Exp;  lines: +3 -2
```

```
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy.

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atprchk.Veqn,v
Working file: verilog/bsrc/at/atprchk.Veqn
head: 1.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;    selected revisions: 1
description:
----------------------------
revision 1.19
date: 1995/04/25 23:07:15;  author: woody;  state: Exp;  lines: +21 -20
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy.

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atxcenbl.pla,v
```

```
Working file: verilog/bsrc/at/atxcenbl.pla
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/25 23:07:17;  author: woody;  state: Exp;  lines: +6 -6
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy.

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/clean-request,v
Working file: verilog/bsrc/at/clean-request
head: 4.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 2
description:
----------------------------
revision 4.10
date: 1995/04/26 18:26:19;  author: woody;  state: Exp;  lines: +1 -0
update placement.
----------------------------
revision 4.9
date: 1995/04/22 17:15:04;  author: dickson;  state: Exp;  lines: +1 -0
solve dc load problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/.checkoutrc,v
Working file: verilog/bsrc/au/.checkoutrc
head: 14.2
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 14.2
date: 1995/04/23 05:44:25;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/BOM,v
Working file: verilog/bsrc/au/BOM
head: 44.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 89;    selected revisions: 4
description:
----------------------------
revision 40.0
date: 1995/04/28 05:25:42;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 39.1
date: 1995/04/28 05:25:35;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 39.0
date: 1995/04/25 06:14:16;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
```

```
----------------------------
revision 38.1
date: 1995/04/25 06:14:08;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/au.power.tab.top,v
Working file: verilog/bsrc/au/au.power.tab.top
head: 16.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 16.10
date: 1995/04/28 04:48:15;  author: tbr;  state: Exp;  lines: +127 -127
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/.checkoutrc,v
Working file: verilog/bsrc/cc/.checkoutrc
head: 9.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 9.3
date: 1995/04/23 05:44:36;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v
Working file: verilog/bsrc/cc/BOM
head: 92.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 82.0
date: 1995/04/28 05:26:08;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs
```

```
ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 81.1
date: 1995/04/28 05:26:01;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 81.0
date: 1995/04/24 11:05:03;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
```

```
----------------------------
revision 80.1
date: 1995/04/24 11:04:56;  author: mws;  state: Exp;  lines: +7 -6
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.power.tab.top,v
Working file: verilog/bsrc/cc/cc.power.tab.top
head: 32.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 32.6
date: 1995/04/28 04:48:20;  author: tbr;  state: Exp;  lines: +343 -335
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/.checkoutrc,v
Working file: verilog/bsrc/cdio/.checkoutrc
head: 19.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 19.9
date: 1995/04/23 05:44:44;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/BOM,v
Working file: verilog/bsrc/cdio/BOM
head: 55.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 110;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 51.0
date: 1995/04/28 05:26:33;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs
```

```
ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 50.1
date: 1995/04/28 05:26:25;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 50.0
date: 1995/04/25 06:14:51;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 49.1
date: 1995/04/25 06:14:43;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/cdio.power.tab.top,v
Working file: verilog/bsrc/cdio/cdio.power.tab.top
head: 34.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 34.9
date: 1995/04/28 04:48:24;  author: tbr;  state: Exp;  lines: +10 -10
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;   selected revisions: 2
description:
```

```
releasebom adding BOM
----------------------------
revision 78.0
date: 1995/04/28 05:26:57;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 77.1
date: 1995/04/28 05:26:50;  author: tbr;  state: Exp;  lines: +14 -13
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/Makefile.gards,v
Working file: verilog/bsrc/ce/Makefile.gards
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 1.14
date: 1995/04/28 00:47:59;  author: vo;  state: Exp;  lines: +11 -46
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .
```

```
cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_cms2ecl.V,v
Working file: verilog/bsrc/ce/ce_cms2ecl.V
head: 2.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 1
description:
----------------------------
revision 2.17
date: 1995/04/28 00:48:02;  author: vo;  state: Exp;  lines: +274 -214
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_flash.V,v
Working file: verilog/bsrc/ce/ce_flash.V
head: 2.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 2
description:
----------------------------
revision 2.18
date: 1995/04/28 00:48:05;  author: vo;  state: Exp;  lines: +150 -124
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .
```

```
cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
----------------------------
revision 2.17
date: 1995/04/26 20:55:39;  author: dickson;  state: Exp;  lines: +4 -2
backdoor rom access not aserting flash rom chip enable signal.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_mck.V,v
Working file: verilog/bsrc/ce/ce_mck.V
head: 32.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 2
description:
----------------------------
revision 32.11
date: 1995/04/28 00:48:07;  author: vo;  state: Exp;  lines: +8 -8
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .
```

```
pimlib.pl,cerberus.cpif: placement to match above changes .
----------------------------
revision 32.10
date: 1995/04/26 02:30:08;  author: dickson;  state: Exp;  lines: +30 -18
made separate sticky flags for hcto 0/1.
added these two flags to machine check details bits as well.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_seg7.V,v
Working file: verilog/bsrc/ce/ce_seg7.V
head: 2.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 2.9
date: 1995/04/28 00:48:09;  author: vo;  state: Exp;  lines: +28 -12
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cecore.V,v
Working file: verilog/bsrc/ce/cecore.V
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 2
description:
----------------------------
revision 1.23
date: 1995/04/28 00:48:11;  author: vo;  state: Exp;  lines: +40 -27
```

...

```
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
----------------------------
revision 1.22
date: 1995/04/26 19:18:41;  author: dickson;  state: Exp;  lines: +5 -2
disable sok_ab0pm function with mltdinhib_abm
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cemaster.V,v
Working file: verilog/bsrc/ce/cemaster.V
head: 1.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17;    selected revisions: 1
description:
----------------------------
revision 1.12
date: 1995/04/28 00:48:14;  author: vo;  state: Exp;  lines: +382 -379
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .
```

```
ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.V,v
Working file: verilog/bsrc/ce/cerberus.V
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 2
description:
----------------------------
revision 1.53
date: 1995/04/28 00:48:16;  author: vo;  state: Exp;  lines: +18 -18
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
----------------------------
revision 1.52
date: 1995/04/26 02:30:11;  author: dickson;  state: Exp;  lines: +5 -4
made separate sticky flags for hcto 0/1.
added these two flags to machine check details bits as well.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.cpif,v
Working file: verilog/bsrc/ce/cerberus.cpif
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 2
description:
```

```
----------------------------
revision 1.27
date: 1995/04/28 01:09:57;  author: vo;  state: Exp;  lines: +11 -10
The last one was out of sync with all the changes .  This one should work better
.
----------------------------
revision 1.26
date: 1995/04/28 00:48:35;  author: vo;  state: Exp;  lines: +7959 -7467
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbskewreg.V,v
Working file: verilog/bsrc/ce/cerbskewreg.V
head: 1.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/04/28 00:48:49;  author: vo;  state: Exp;  lines: +3 -3
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .
```

```
ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbtest.V,v
Working file: verilog/bsrc/ce/cerbtest.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
----------------------------
revision 1.40
date: 1995/04/28 00:48:52;  author: vo;  state: Exp;  lines: +3 -2
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ceregcore.V,v
Working file: verilog/bsrc/ce/ceregcore.V
head: 1.44
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 44;    selected revisions: 2
description:
----------------------------
```

```
revision 1.40
date: 1995/04/28 00:48:56;  author: vo;  state: Exp;  lines: +3 -3
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .

cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
----------------------------
revision 1.39
date: 1995/04/26 02:30:13;  author: dickson;  state: Exp;  lines: +7 -5
made separate sticky flags for hcto 0/1.
added these two flags to machine check details bits as well.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/pimlib.pl,v
Working file: verilog/bsrc/ce/pimlib.pl
head: 77.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 3
description:
----------------------------
revision 77.3
date: 1995/04/28 00:48:58;  author: vo;  state: Exp;  lines: +286 -70
Makefile.gards : Removed more obsolete rules .
Used a different delay equation .  The old one converted wire load to
to an equivalent transistor fanout .  The new one converted load to ff .

cerberus.V : changed all module names from uxx to something closer to
the module name .

ce_cms2ecl.V ce_flash.V ce_seg7.V cemaster.V : lots of fanout related changes .
Renamed instances to facilitate placement script coding .

ce_mck.V : moved converters to further reduce wires  throgh lhs choke point .
added buffer .

ce_core.V : retuned the main clock .  Fixed a few more slow nodes .
```

```
cerbskewreg.V : Fixed a few more slow nodes (we have lots of them here) .

ceregcore.V: buffered sorom .

cerbtest.V : printed octlet address , added time limit .

pimlib.pl,cerberus.cpif: placement to match above changes .
----------------------------
revision 77.2
date: 1995/04/26 01:17:59;  author: vo;  state: Exp;  lines: +91 -13
saved it or lose it .
----------------------------
revision 77.1
date: 1995/04/25 20:29:58;  author: vo;  state: Exp;
perl script to aid cerberus placement .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cg/BOM,v
Working file: verilog/bsrc/cg/BOM
head: 11.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 11.0
date: 1995/04/24 17:14:33;  author: vo;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cg

added cgclockbias.sp to list of things to make
----------------------------
revision 10.1
date: 1995/04/24 17:14:26;  author: vo;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cg/Makefile,v
Working file: verilog/bsrc/cg/Makefile
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 1.9
date: 1995/04/24 17:03:17;  author: vo;  state: Exp;  lines: +2 -2
added cgclockbias.sp to list of things to make
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/.checkoutrc,v
Working file: verilog/bsrc/cj/.checkoutrc
```

```
head: 46.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 46.5
date: 1995/04/23 05:44:54;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/BOM,v
Working file: verilog/bsrc/cj/BOM
head: 122.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 259;   selected revisions: 6
description:
----------------------------
revision 116.0
date: 1995/04/28 05:27:33;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 115.1
date: 1995/04/28 05:27:25;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 115.0
date: 1995/04/26 08:32:50;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
```

```
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 114.1
date: 1995/04/26 08:32:42;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 114.0
date: 1995/04/24 11:05:43;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
```

```
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 113.1
date: 1995/04/24 11:05:36;  author: mws;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cj.V,v
Working file: verilog/bsrc/cj/cj.V
head: 1.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
Cmos Icache glue logic unit.  Mostly intended to abut against custom array.
----------------------------
revision 1.21
date: 1995/04/24 10:29:12;  author: mws;  state: Exp;  lines: +1 -11
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cj.pim,v
Working file: verilog/bsrc/cj/cj.pim
head: 62.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 62.9
date: 1995/04/24 10:29:14;  author: mws;  state: Exp;  lines: +4 -4
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
```

```
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cj.power.tab.top,v
Working file: verilog/bsrc/cj/cj.power.tab.top
head: 69.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 69.12
date: 1995/04/28 04:48:29;  author: tbr;  state: Exp;  lines: +15 -23
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cjrst.tst,v
Working file: verilog/bsrc/cj/cjrst.tst
head: 13.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 1
description:
----------------------------
revision 13.36
date: 1995/04/26 08:20:32;  author: mws;  state: Exp;  lines: +4 -4
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/rsrvd.tst,v
Working file: verilog/bsrc/cj/rsrvd.tst
head: 78.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 78.10
date: 1995/04/24 10:29:15;  author: mws;  state: Exp;  lines: +3 -3
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
```

```
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
==============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ck/.checkoutrc,v
Working file: verilog/bsrc/ck/.checkoutrc
head: 10.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 10.4
date: 1995/04/23 05:45:03;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
==============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ck/BOM,v
Working file: verilog/bsrc/ck/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 26.0
date: 1995/04/28 05:28:00;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement
```

```
update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 25.1
date: 1995/04/28 05:27:52;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 25.0
date: 1995/04/25 06:15:41;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 24.1
date: 1995/04/25 06:15:34;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ck/ck.power.tab.top,v
Working file: verilog/bsrc/ck/ck.power.tab.top
head: 17.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 17.8
date: 1995/04/28 04:48:33;  author: tbr;  state: Exp;  lines: +35 -35
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/.checkoutrc,v
Working file: verilog/bsrc/cp/.checkoutrc
head: 9.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 9.4
date: 1995/04/23 05:45:11;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
```

```
head: 60.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119;   selected revisions: 11
description:
releasebom adding BOM
----------------------------
revision 54.0
date: 1995/04/28 05:28:27;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 53.1
date: 1995/04/28 05:28:18;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 53.0
date: 1995/04/26 08:33:15;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
```

```
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 52.1
date: 1995/04/26 08:33:08;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 52.0
date: 1995/04/25 23:10:56;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy. *not complete*

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.

placement updates to follow.
CVS: ----------------------------------------------------------------------
CVS: Enter Log.  Lines beginning with `CVS: ' are removed automatically
CVS:
CVS: Committing in
CVS:
CVS: Modified Files:
CVS:  euterpe.V
CVS: ----------------------------------------------------------------------
----------------------------
revision 51.2
date: 1995/04/25 23:10:48;  author: woody;  state: Exp;  lines: +1 -1
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 51.1
date: 1995/04/25 20:24:48;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
----------------------------
revision 51.0
date: 1995/04/25 06:16:08;  author: tbr;  state: Exp;  lines: +1 -1
```

```
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 50.1
date: 1995/04/25 06:15:59;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 50.0
date: 1995/04/24 11:06:09;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
```

```
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 49.1
date: 1995/04/24 11:06:03;  author: mws;  state: Exp;  lines: +8 -8
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/Makefile,v
Working file: verilog/bsrc/cp/Makefile
head: 1.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 1.9
date: 1995/04/24 10:58:35;  author: mws;  state: Exp;  lines: +2 -2
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.V,v
Working file: verilog/bsrc/cp/cp.V
head: 1.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 2
description:
----------------------------
revision 1.34
date: 1995/04/25 20:24:15;  author: mws;  state: Exp;  lines: +2 -2
Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
----------------------------
revision 1.33
```

```
date: 1995/04/24 10:58:37;  author: mws;  state: Exp;  lines: +190 -400
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.pim,v
Working file: verilog/bsrc/cp/cp.pim
head: 7.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 7.14
date: 1995/04/24 10:58:39;  author: mws;  state: Exp;  lines: +7 -7
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.power.tab.top,v
Working file: verilog/bsrc/cp/cp.power.tab.top
head: 19.12
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 3
description:
----------------------------
revision 19.11
date: 1995/04/28 04:48:36;  author: tbr;  state: Exp;  lines: +357 -403
update all power.tab.top files from bom 288.0
----------------------------
revision 19.10
date: 1995/04/28 00:50:33;  author: mws;  state: Exp;  lines: +8 -8
  Make uu/UetaOutUT/u2, cp/itw05/u0, cp/itr01/u0, cp/ibw05/u0, cp/ibr01/u0
  half swing and cut power about in half, rounded up.
----------------------------
revision 19.9
date: 1995/04/24 10:58:41;  author: mws;  state: Exp;  lines: +12 -12
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cph.pim,v
Working file: verilog/bsrc/cp/cph.pim
head: 41.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 41.6
date: 1995/04/24 10:58:43;  author: mws;  state: Exp;  lines: +1 -1
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
```

```
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cpl.pim,v
Working file: verilog/bsrc/cp/cpl.pim
head: 41.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 41.5
date: 1995/04/24 10:58:45;  author: mws;  state: Exp;  lines: +82 -64
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/power.tab.local,v
Working file: verilog/bsrc/cp/power.tab.local
head: 5.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 2
description:
----------------------------
revision 5.12
date: 1995/04/25 00:45:19;  author: dickson;  state: Exp;  lines: +3 -1
fix csyn error for oload ostore
```

```
----------------------------
revision 5.11
date: 1995/04/25 00:32:27;  author: dickson;  state: Exp;  lines: +113 -1
fix csyn errors
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/BOM,v
Working file: verilog/bsrc/ctiod/BOM
head: 31.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 61;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 27.0
date: 1995/04/28 05:28:56;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 26.1
date: 1995/04/28 05:28:47;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/ctiod.power.tab.top,v
Working file: verilog/bsrc/ctiod/ctiod.power.tab.top
head: 12.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 12.8
date: 1995/04/28 04:48:40;  author: tbr;  state: Exp;  lines: +57 -57
update all power.tab.top files from bom 288.0
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/.checkoutrc,v
Working file: verilog/bsrc/ctioi/.checkoutrc
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/04/23 05:45:19;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/BOM,v
Working file: verilog/bsrc/ctioi/BOM
head: 28.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 56;    selected revisions: 6
description:
releasebom adding BOM
----------------------------
revision 27.0
date: 1995/04/28 05:29:22;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 26.1
date: 1995/04/28 05:29:14;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 26.0
date: 1995/04/25 06:16:55;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.
```

```
Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 25.1
date: 1995/04/25 06:16:45;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 25.0
date: 1995/04/24 11:06:35;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 24.3
date: 1995/04/24 11:06:29;  author: mws;  state: Exp;  lines: +3 -3
```

```
releasebom: File needs to be up-to-date to use commit -r
===================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/ctioi.V,v
Working file: verilog/bsrc/ctioi/ctioi.V
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 1.16
date: 1995/04/24 10:43:15;  author: mws;  state: Exp;  lines: +3 -14
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
===================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/ctioi.pim,v
Working file: verilog/bsrc/ctioi/ctioi.pim
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 1.9
date: 1995/04/24 10:43:17;  author: mws;  state: Exp;  lines: +4 -4
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/ctioi.power.tab.top,v
Working file: verilog/bsrc/ctioi/ctioi.power.tab.top
head: 9.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 9.9
date: 1995/04/28 04:48:44;  author: tbr;  state: Exp;  lines: +103 -115
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/power.tab.local,v
Working file: verilog/bsrc/ctioi/power.tab.local
head: 4.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 4.6
date: 1995/04/24 21:15:50;  author: dickson;  state: Exp;  lines: +72 -0
fix csyn error
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/BOM,v
Working file: verilog/bsrc/dr/BOM
head: 77.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 155;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 72.0
date: 1995/04/28 05:30:17;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes
```

```
nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 71.1
date: 1995/04/28 05:30:10;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 71.0
date: 1995/04/25 06:18:25;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 70.1
date: 1995/04/25 06:18:17;  author: tbr;  state: Exp;  lines: +8 -7
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/Makefile,v
Working file: verilog/bsrc/dr/Makefile
head: 1.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 34;    selected revisions: 1
description:
----------------------------
revision 1.32
date: 1995/04/22 16:04:33;  author: billz;  state: Exp;  lines: +2 -2
Solves DC load disturbance.  But doesn't converge in 2 iterations.
But it's got a lot of other great stuff going for it, so i'll
check it in and concurrently let it iterate more.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/dr.V,v
Working file: verilog/bsrc/dr/dr.V
head: 1.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 1.25
```

```
date: 1995/04/22 16:04:35;  author: billz;  state: Exp;  lines: +3 -3
Solves DC load disturbance.  But doesn't converge in 2 iterations.
But it's got a lot of other great stuff going for it, so i'll
check it in and concurrently let it iterate more.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/dr.power.tab.top,v
Working file: verilog/bsrc/dr/dr.power.tab.top
head: 43.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 43.6
date: 1995/04/28 04:48:51;  author: tbr;  state: Exp;  lines: +755 -751
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/drbank.V,v
Working file: verilog/bsrc/dr/drbank.V
head: 7.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 7.11
date: 1995/04/22 16:04:38;  author: billz;  state: Exp;  lines: +5 -3
Solves DC load disturbance.  But doesn't converge in 2 iterations.
But it's got a lot of other great stuff going for it, so i'll
check it in and concurrently let it iterate more.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/drbanksel.custom.pim,v
Working file: verilog/bsrc/dr/drbanksel.custom.pim
head: 64.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 64.2
date: 1995/04/22 16:04:39;  author: billz;  state: Exp;  lines: +2 -2
Solves DC load disturbance.  But doesn't converge in 2 iterations.
But it's got a lot of other great stuff going for it, so i'll
check it in and concurrently let it iterate more.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/drcontroljunk.pim,v
Working file: verilog/bsrc/dr/drcontroljunk.pim
```

```
head: 70.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 70.1
date: 1995/04/22 16:04:42;  author: billz;  state: Exp;
Solves DC load disturbance.  But doesn't converge in 2 iterations.
But it's got a lot of other great stuff going for it, so i'll
check it in and concurrently let it iterate more.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/genpim.pl,v
Working file: verilog/bsrc/dr/genpim.pl
head: 20.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 20.12
date: 1995/04/22 16:04:43;  author: billz;  state: Exp;  lines: +1 -5
Solves DC load disturbance.  But doesn't converge in 2 iterations.
But it's got a lot of other great stuff going for it, so i'll
check it in and concurrently let it iterate more.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/pimlib.pl,v
Working file: verilog/bsrc/dr/pimlib.pl
head: 20.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 20.15
date: 1995/04/22 16:04:45;  author: billz;  state: Exp;  lines: +6 -4
Solves DC load disturbance.  But doesn't converge in 2 iterations.
But it's got a lot of other great stuff going for it, so i'll
check it in and concurrently let it iterate more.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/.checkoutrc,v
Working file: verilog/bsrc/drio/.checkoutrc
head: 3.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
```

```
description:
----------------------------
revision 3.5
date: 1995/04/23 05:45:38;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/BOM,v
Working file: verilog/bsrc/drio/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 20.0
date: 1995/04/28 05:30:38;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 19.1
date: 1995/04/28 05:30:31;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 19.0
date: 1995/04/25 06:18:56;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 18.1
```

```
date: 1995/04/25 06:18:48;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/drio.power.tab.top,v
Working file: verilog/bsrc/drio/drio.power.tab.top
head: 9.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 9.8
date: 1995/04/28 04:48:59;  author: tbr;  state: Exp;  lines: +22 -22
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/.checkoutrc,v
Working file: verilog/bsrc/es/.checkoutrc
head: 45.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 45.2
date: 1995/04/23 05:45:47;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;   selected revisions: 6
description:
----------------------------
revision 89.0
date: 1995/04/28 05:30:58;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
```

```
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 88.1
date: 1995/04/28 05:30:52;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 88.0
date: 1995/04/25 06:19:28;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 87.1
date: 1995/04/25 06:19:20;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 87.0
date: 1995/04/22 17:23:25;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

solve dc load problem
----------------------------
revision 86.1
date: 1995/04/22 17:23:18;  author: dickson;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.power.tab.top,v
Working file: verilog/bsrc/es/es.power.tab.top
head: 65.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 65.11
date: 1995/04/28 04:49:13;  author: tbr;  state: Exp;  lines: +2145 -2127
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/.checkoutrc,v
Working file: verilog/bsrc/gf/.checkoutrc
```

```
head: 11.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 11.4
date: 1995/04/23 05:45:55;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/BOM,v
Working file: verilog/bsrc/gf/BOM
head: 37.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 33.0
date: 1995/04/28 05:31:19;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 32.1
date: 1995/04/28 05:31:13;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 32.0
date: 1995/04/25 06:19:53;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.
```

```
New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 31.1
date: 1995/04/25 06:19:45;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.power.tab.top,v
Working file: verilog/bsrc/gf/gf.power.tab.top
head: 19.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 19.9
date: 1995/04/28 04:49:30;  author: tbr;  state: Exp;  lines: +234 -230
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;   selected revisions: 10
description:
releasebom adding BOM
----------------------------
revision 89.0
date: 1995/04/28 05:31:42;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 88.1
```

]

```
date: 1995/04/28 05:31:36;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 88.0
date: 1995/04/27 21:11:29;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt

gt/pimlib.pl:  Move tau1[ab] drivers from the left side to the right side so
  that they will be near clumped loads to fix dcload violation.
----------------------------
revision 87.1
date: 1995/04/27 21:11:22;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 87.0
date: 1995/04/25 02:49:45;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt

euterpe.status gt/gtsnake.V gt/pimlib.pl:
  Convert full- to half-swing load on busy toplevel net UUetaUTR11.
----------------------------
revision 86.1
date: 1995/04/25 02:49:37;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 86.0
date: 1995/04/25 01:47:48;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt

gt/gt.V gt/genpim.pl gt/pimlib.pl:  Add dedicated tau for 107uA GTLB.
  Move tau0a & tau0b drivers from genpim.pl to pimlib.pl's miscstuff subroutine
  and get on proper row.
gt/genptab.pl:  dickson fix csyn error; geert removed UgvaR8R9[ab] power set.
----------------------------
revision 85.1
date: 1995/04/25 01:47:39;  author: mws;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 85.0
date: 1995/04/23 03:57:31;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt

solve dc load problems
----------------------------
revision 84.1
date: 1995/04/23 03:57:25;  author: dickson;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/Makefile,v
Working file: verilog/bsrc/gt/Makefile
head: 1.29
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 29;    selected revisions: 1
```

```
description:
----------------------------
revision 1.28
date: 1995/04/23 03:56:47;  author: dickson;  state: Exp;  lines: +3 -1
solve dc load problem.
i kludged it tim. i added an explicit placement of two
cells in genpim.pl : )
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/clean-request,v
Working file: verilog/bsrc/gt/clean-request
head: 41.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 41.7
date: 1995/04/23 03:56:48;  author: dickson;  state: Exp;  lines: +2 -1
solve dc load problem.
i kludged it tim. i added an explicit placement of two
cells in genpim.pl : )
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/genpim.pl,v
Working file: verilog/bsrc/gt/genpim.pl
head: 26.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
----------------------------
revision 26.8
date: 1995/04/25 01:45:02;  author: mws;  state: Exp;  lines: +1 -4
gt/gt.V gt/genpim.pl gt/pimlib.pl:  Add dedicated tau for 107uA GTLB.
  Move tau0a & tau0b drivers from genpim.pl to pimlib.pl's miscstuff subroutine
  and get on proper row.
----------------------------
revision 26.7
date: 1995/04/23 03:56:50;  author: dickson;  state: Exp;  lines: +5 -1
solve dc load problem.
i kludged it tim. i added an explicit placement of two
cells in genpim.pl : )
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/genptab.pl,v
Working file: verilog/bsrc/gt/genptab.pl
head: 24.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
```

```
description:
----------------------------
revision 24.6
date: 1995/04/24 21:15:32;  author: dickson;  state: Exp;  lines: +14 -1
fix csyn error
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gt.V,v
Working file: verilog/bsrc/gt/gt.V
head: 2.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 2.25
date: 1995/04/25 01:45:04;  author: mws;  state: Exp;  lines: +22 -11
gt/gt.V gt/genpim.pl gt/pimlib.pl:  Add dedicated tau for 107uA GTLB.
  Move tau0a & tau0b drivers from genpim.pl to pimlib.pl's miscstuff subroutine
  and get on proper row.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gt.power.tab.top,v
Working file: verilog/bsrc/gt/gt.power.tab.top
head: 54.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 54.9
date: 1995/04/28 04:49:36;  author: tbr;  state: Exp;  lines: +321 -313
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gtsnake.V,v
Working file: verilog/bsrc/gt/gtsnake.V
head: 7.41
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 41;    selected revisions: 1
description:
----------------------------
revision 7.39
date: 1995/04/25 02:45:59;  author: mws;  state: Exp;  lines: +2 -2
euterpe.status gt/gtsnake.V gt/pimlib.pl:
  Convert full- to half-swing load on busy toplevel net UUetaUTR11.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/pimlib.pl,v
Working file: verilog/bsrc/gt/pimlib.pl
```

```
head: 26.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 4
description:
----------------------------
revision 26.20
date: 1995/04/27 21:10:52;  author: mws;  state: Exp;  lines: +3 -3
Move tau1[ab] drivers from the left side to the right side so
  that they will be near clumped loads to fix dcload violation.
----------------------------
revision 26.19
date: 1995/04/25 02:46:02;  author: mws;  state: Exp;  lines: +2 -1
euterpe.status gt/gtsnake.V gt/pimlib.pl:
  Convert full- to half-swing load on busy toplevel net UUetaUTR11.
----------------------------
revision 26.18
date: 1995/04/25 01:45:07;  author: mws;  state: Exp;  lines: +4 -1
gt/gt.V gt/genpim.pl gt/pimlib.pl:  Add dedicated tau for 107uA GTLB.
  Move tau0a & tau0b drivers from genpim.pl to pimlib.pl's miscstuff subroutine
  and get on proper row.
----------------------------
revision 26.17
date: 1995/04/23 03:56:51;  author: dickson;  state: Exp;  lines: +3 -3
solve dc load problem.
i kludged it tim. i added an explicit placement of two
cells in genpim.pl : )
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 105.0
date: 1995/04/28 05:32:04;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes
```

```
nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 104.1
date: 1995/04/28 05:31:57;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0.power.tab.top,v
Working file: verilog/bsrc/hc/hc0.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 68.7
date: 1995/04/28 04:49:43;  author: tbr;  state: Exp;  lines: +3280 -350
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc1.power.tab.top,v
Working file: verilog/bsrc/hc/hc1.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 68.8
date: 1995/04/28 04:49:51;  author: tbr;  state: Exp;  lines: +2936 -0
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/.checkoutrc,v
Working file: verilog/bsrc/hz/.checkoutrc
head: 4.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 4.3
date: 1995/04/23 05:46:07;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/BOM,v
Working file: verilog/bsrc/hz/BOM
```

```
head: 30.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 58;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 28.0
date: 1995/04/28 05:32:24;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 27.1
date: 1995/04/28 05:32:18;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 27.0
date: 1995/04/24 11:08:00;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
```

```
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 26.1
date: 1995/04/24 07:38:59;  author: mws;  state: Exp;  lines: +5 -5
Release Target: euterpe/verilog/bsrc/hz

{icc,ife,hz}/.checkoutrc:  gards_display no longer necessary
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need hrbuf in GT just for GTLB (it+others too heavy for far away hz).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/hz.V,v
Working file: verilog/bsrc/hz/hz.V
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 1.14
date: 1995/04/24 07:36:38;  author: mws;  state: Exp;  lines: +2 -4
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need hrbuf in GT just for GTLB (it+others too heavy for far away hz).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/hz.pim,v
Working file: verilog/bsrc/hz/hz.pim
head: 9.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 9.8
date: 1995/04/24 07:36:40;  author: mws;  state: Exp;  lines: +2 -2
```

```
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need hrbuf in GT just for GTLB (it+others too heavy for far away hz).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/hz.power.tab.top,v
Working file: verilog/bsrc/hz/hz.power.tab.top
head: 10.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
----------------------------
revision 10.8
date: 1995/04/28 04:49:57;  author: tbr;  state: Exp;  lines: +29 -29
update all power.tab.top files from bom 288.0
----------------------------
revision 10.7
date: 1995/04/24 07:36:42;  author: mws;  state: Exp;  lines: +2 -4
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need hrbuf in GT just for GTLB (it+others too heavy for far away hz).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 44.0
date: 1995/04/28 05:32:43;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 43.1
date: 1995/04/28 05:32:37;  author: tbr;  state: Exp;  lines: +2 -2
```

```
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 43.0
date: 1995/04/24 11:08:19;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 42.1
date: 1995/04/24 11:08:13;  author: mws;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.V,v
Working file: verilog/bsrc/icc/icc.V
head: 1.45
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 45;    selected revisions: 1
description:
----------------------------
revision 1.43
date: 1995/04/24 10:54:39;  author: mws;  state: Exp;  lines: +17 -11
icc/icc.V icc/icc.pim.txt:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.pim.txt,v
Working file: verilog/bsrc/icc/icc.pim.txt
head: 39.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 39.3
date: 1995/04/24 10:54:41;  author: mws;  state: Exp;  lines: +30 -30
icc/icc.V icc/icc.pim.txt:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.power.tab.top,v
Working file: verilog/bsrc/icc/icc.power.tab.top
head: 19.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 19.7
date: 1995/04/28 04:50:00;  author: tbr;  state: Exp;  lines: +944 -454
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc_control.pim,v
Working file: verilog/bsrc/icc/icc_control.pim
head: 16.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
```

```
revision 16.15
date: 1995/04/24 10:54:42;  author: mws;  state: Exp;  lines: +2 -1
icc/icc.V icc/icc.pim.txt:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/BOM,v
Working file: verilog/bsrc/ife/BOM
head: 68.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 140;   selected revisions: 6
description:
----------------------------
revision 66.0
date: 1995/04/28 05:33:03;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 65.1
date: 1995/04/28 05:32:57;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 65.0
date: 1995/04/26 08:35:12;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
```

```
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 64.1
date: 1995/04/26 08:35:06;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 64.0
date: 1995/04/24 11:08:42;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
```

```
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 63.1
date: 1995/04/24 11:08:35;  author: mws;  state: Exp;  lines: +5 -7
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife.V,v
Working file: verilog/bsrc/ife/ife.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
----------------------------
revision 1.45
date: 1995/04/24 10:55:55;  author: mws;  state: Exp;  lines: +26 -4
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife.pim.txt,v
Working file: verilog/bsrc/ife/ife.pim.txt
head: 61.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 61.2
date: 1995/04/24 10:55:57;  author: mws;  state: Exp;  lines: +30 -30
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
```

```
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife.power.tab.top,v
Working file: verilog/bsrc/ife/ife.power.tab.top
head: 40.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 40.5
date: 1995/04/28 04:50:05;  author: tbr;  state: Exp;  lines: +363 -1035
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ife_control.pim,v
Working file: verilog/bsrc/ife/ife_control.pim
head: 15.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 15.14
date: 1995/04/24 10:55:59;  author: mws;  state: Exp;  lines: +1 -913
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ifrst.tst,v
Working file: verilog/bsrc/ife/ifrst.tst
head: 2.12
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 2.11
date: 1995/04/26 08:17:05;  author: mws;  state: Exp;  lines: +2 -2
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/.checkoutrc,v
Working file: verilog/bsrc/io/.checkoutrc
head: 9.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 9.6
date: 1995/04/23 05:46:16;  author: tbr;  state: Exp;  lines: +3 -3
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/BOM,v
Working file: verilog/bsrc/io/BOM
head: 48.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 94;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 43.0
date: 1995/04/28 05:33:23;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 286 top level
----------------------------
revision 42.1
```

```
date: 1995/04/28 05:33:17;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 42.0
date: 1995/04/25 06:21:11;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 41.1
date: 1995/04/25 06:21:03;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/io0.power.tab.top,v
Working file: verilog/bsrc/io/io0.power.tab.top
head: 24.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 24.8
date: 1995/04/28 04:50:10;  author: tbr;  state: Exp;  lines: +957 -49
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/io1.power.tab.top,v
Working file: verilog/bsrc/io/io1.power.tab.top
head: 24.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 24.8
date: 1995/04/28 04:50:13;  author: tbr;  state: Exp;  lines: +961 -53
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/.checkoutrc,v
Working file: verilog/bsrc/iq/.checkoutrc
head: 22.4
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 22.4
date: 1995/04/23 05:46:26;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/BOM,v
Working file: verilog/bsrc/iq/BOM
head: 67.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 145;   selected revisions: 6
description:
----------------------------
revision 66.0
date: 1995/04/28 05:33:44;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 65.1
date: 1995/04/28 05:33:37;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 65.0
date: 1995/04/27 00:15:03;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
iq/iq.V:  Remove dead predGoQ5 wire decl.
euterpe.status:  Over the last few BOMs:
  fullswing cb4 input to gtsnake (UUetaUTR11[2]) was fixed to halfswing,
```

```
  broken SMUX instructions were made reserved a few BOMs ago,
  ITag data out was reduced from hr to flop in choke corridor,
  ICC bus into ITag data in reg was made psuedo-diff in choke corridor.
----------------------------
revision 64.1
date: 1995/04/27 00:14:53;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 64.0
date: 1995/04/25 06:21:35;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 63.1
date: 1995/04/25 06:21:28;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/iq.V,v
Working file: verilog/bsrc/iq/iq.V
head: 1.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 1
description:
instruction queue unit
----------------------------
revision 1.33
date: 1995/04/26 23:57:04;  author: mws;  state: Exp;  lines: +1 -2
iq/iq.V:  Remove dead predGoQ5 wire decl.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/iq/iq.power.tab.top,v
Working file: verilog/bsrc/iq/iq.power.tab.top
head: 50.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 50.6
date: 1995/04/28 04:50:18;  author: tbr;  state: Exp;  lines: +37 -37
update all power.tab.top files from bom 288.0
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/.checkoutrc,v
Working file: verilog/bsrc/lt/.checkoutrc
head: 56.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 56.2
date: 1995/04/23 05:46:36;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/BOM,v
Working file: verilog/bsrc/lt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 196;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 93.0
date: 1995/04/28 05:34:04;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 92.1
date: 1995/04/28 05:33:57;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 92.0
date: 1995/04/25 06:21:58;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.
```

```
Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 91.1
date: 1995/04/25 06:21:51;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt.power.tab.top,v
Working file: verilog/bsrc/lt/lt.power.tab.top
head: 68.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 68.11
date: 1995/04/28 04:50:23;  author: tbr;  state: Exp;  lines: +183 -261
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/.checkoutrc,v
Working file: verilog/bsrc/mc/.checkoutrc
head: 17.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 17.4
date: 1995/04/23 05:46:46;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/BOM,v
Working file: verilog/bsrc/mc/BOM
head: 79.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 157;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 70.0
date: 1995/04/28 05:34:25;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 69.1
date: 1995/04/28 05:34:18;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 69.0
date: 1995/04/25 06:22:19;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 68.1
date: 1995/04/25 06:22:12;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.power.tab.top,v
Working file: verilog/bsrc/mc/mc.power.tab.top
head: 37.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 37.9
date: 1995/04/28 04:50:31;  author: tbr;  state: Exp;  lines: +703 -703
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mg/BOM,v
Working file: verilog/bsrc/mg/BOM
```

```
head: 51.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 117;   selected revisions: 2
description:
----------------------------
revision 51.0
date: 1995/04/26 08:35:59;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 50.1
date: 1995/04/26 08:35:53;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mg/mgrst.tst,v
Working file: verilog/bsrc/mg/mgrst.tst
head: 8.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 8.28
date: 1995/04/26 08:23:35;  author: mws;  state: Exp;  lines: +2 -1
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/.checkoutrc,v
```

```
Working file: verilog/bsrc/mst/.checkoutrc
head: 13.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 13.3
date: 1995/04/23 05:46:54;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/BOM,v
Working file: verilog/bsrc/mst/BOM
head: 38.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 74;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 38.0
date: 1995/04/28 05:34:51;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 37.1
date: 1995/04/28 05:34:44;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 37.0
date: 1995/04/24 03:25:13;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/mst

solve dc load problems
----------------------------
revision 36.1
date: 1995/04/24 03:25:07;  author: dickson;  state: Exp;  lines: +10 -10
```

```
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/Makefile,v
Working file: verilog/bsrc/mst/Makefile
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 1.16
date: 1995/04/24 03:24:16;  author: dickson;  state: Exp;  lines: +3 -1
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/clean-request,v
Working file: verilog/bsrc/mst/clean-request
head: 13.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 13.10
date: 1995/04/24 03:24:17;  author: dickson;  state: Exp;  lines: +2 -1
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/msbooth.V,v
Working file: verilog/bsrc/mst/msbooth.V
head: 1.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 1.6
date: 1995/04/24 03:24:19;  author: dickson;  state: Exp;  lines: +36 -43
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/mscsadd16a.V,v
Working file: verilog/bsrc/mst/mscsadd16a.V
head: 20.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
```

```
----------------------------
revision 20.2
date: 1995/04/24 03:24:20;  author: dickson;  state: Exp;  lines: +15 -15
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/mscsadd16b.V,v
Working file: verilog/bsrc/mst/mscsadd16b.V
head: 20.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 20.2
date: 1995/04/24 03:24:21;  author: dickson;  state: Exp;  lines: +15 -15
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/mscsadd16e.V,v
Working file: verilog/bsrc/mst/mscsadd16e.V
head: 20.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 20.2
date: 1995/04/24 03:24:23;  author: dickson;  state: Exp;  lines: +15 -15
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/msrcd16.V,v
Working file: verilog/bsrc/mst/msrcd16.V
head: 20.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 20.2
date: 1995/04/24 03:24:24;  author: dickson;  state: Exp;  lines: +84 -52
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/mst.pim,v
Working file: verilog/bsrc/mst/mst.pim
head: 2.18
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
----------------------------
revision 2.18
date: 1995/04/24 03:24:29;  author: dickson;  state: Exp;  lines: +448 -0
solve dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mst/mst.power.tab.top,v
Working file: verilog/bsrc/mst/mst.power.tab.top
head: 23.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 23.9
date: 1995/04/28 04:50:44;  author: tbr;  state: Exp;  lines: +1629 -789
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v
Working file: verilog/bsrc/nb/BOM
head: 130.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 261;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 123.0
date: 1995/04/28 05:35:20;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 122.1
date: 1995/04/28 05:35:13;  author: tbr;  state: Exp;  lines: +3 -4
```

```
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nb.power.tab.top,v
Working file: verilog/bsrc/nb/nb.power.tab.top
head: 82.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 82.9
date: 1995/04/28 04:51:03;  author: tbr;  state: Exp;  lines: +836 -838
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nb_mid.pim,v
Working file: verilog/bsrc/nb/nb_mid.pim
head: 88.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 88.15
date: 1995/04/26 16:43:41;  author: billz;  state: Exp;  lines: +3 -2
Attempts to fix the problem of nbwed/unbwed/u0 sticking out and
displacing the datapath portion of nb to the right.  Just moved
this cell up 4 rows.  nb_control.pim is removed because it is
not used in the present placement.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/.checkoutrc,v
Working file: verilog/bsrc/rg/.checkoutrc
head: 60.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 60.3
date: 1995/04/23 05:47:08;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 297;   selected revisions: 12
description:
----------------------------
revision 122.0
date: 1995/04/28 06:30:49;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

try and avoid collisions in top level
----------------------------
revision 121.1
date: 1995/04/28 06:30:42;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 121.0
date: 1995/04/28 05:35:54;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 120.1
date: 1995/04/28 05:35:47;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 120.0
date: 1995/04/26 08:36:51;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnfIctI3 CJciCnfIctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
```

```
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 119.1
date: 1995/04/26 08:36:44;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 119.0
date: 1995/04/25 06:23:29;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 118.1
date: 1995/04/25 06:23:21;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 118.0
date: 1995/04/24 11:10:05;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
```

```
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 117.1
date: 1995/04/24 11:09:58;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 117.0
date: 1995/04/22 23:32:39;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

fix dc load problem
----------------------------
revision 116.1
date: 1995/04/22 23:32:33;  author: dickson;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/clean-request,v
Working file: verilog/bsrc/rg/clean-request
head: 60.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 2
description:
----------------------------
revision 60.10
date: 1995/04/28 06:29:50;  author: dickson;  state: Exp;  lines: +1 -0
try and avoid collisions at top level
----------------------------
revision 60.9
date: 1995/04/22 23:31:56;  author: dickson;  state: Exp;  lines: +1 -0
fix dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 2
description:
----------------------------
revision 82.21
date: 1995/04/28 06:29:53;  author: dickson;  state: Exp;  lines: +232 -234
try and avoid collisions at top level
----------------------------
revision 82.20
date: 1995/04/22 23:31:59;  author: dickson;  state: Exp;  lines: +3 -0
fix dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.power.tab.top,v
Working file: verilog/bsrc/rg/rg.power.tab.top
head: 79.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 79.10
date: 1995/04/28 04:51:22;  author: tbr;  state: Exp;  lines: +268 -262
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg_control.pim,v
Working file: verilog/bsrc/rg/rg_control.pim
head: 67.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 67.4
date: 1995/04/24 10:40:17;  author: mws;  state: Exp;  lines: +3 -242
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rgcr.V,v
Working file: verilog/bsrc/rg/rgcr.V
head: 1.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 1.12
```

. . . .

```
date: 1995/04/22 23:32:01;  author: dickson;  state: Exp;  lines: +7 -3
fix dc load problems
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rgpc.V,v
Working file: verilog/bsrc/rg/rgpc.V
head: 1.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 1
description:
PC (program counter) address path.
Intended to go in the main data path with rgdp.V.
----------------------------
revision 1.33
date: 1995/04/25 02:46:58;  author: mws;  state: Exp;  lines: +3 -4
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rgrst.tst,v
Working file: verilog/bsrc/rg/rgrst.tst
head: 9.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 9.27
date: 1995/04/26 08:22:53;  author: mws;  state: Exp;  lines: +2 -2
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/.checkoutrc,v
Working file: verilog/bsrc/rgxmit/.checkoutrc
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/04/23 05:47:16;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/BOM,v
Working file: verilog/bsrc/rgxmit/BOM
head: 42.0
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 82;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 42.0
date: 1995/04/28 05:36:16;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 41.1
date: 1995/04/28 05:36:09;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 41.0
date: 1995/04/24 11:10:26;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cp1.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cp1.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
```

. . .

```
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 40.1
date: 1995/04/24 11:10:19;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/rgxmit.power.tab.top,v
Working file: verilog/bsrc/rgxmit/rgxmit.power.tab.top
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 19.6
date: 1995/04/28 04:51:30;  author: tbr;  state: Exp;  lines: +38 -42
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rgxmit/rgxmit_control.pim,v
Working file: verilog/bsrc/rgxmit/rgxmit_control.pim
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 1.16
date: 1995/04/24 10:39:33;  author: mws;  state: Exp;  lines: +3 -2
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/BOM,v
Working file: verilog/bsrc/sr/BOM
head: 75.0
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 65.0
date: 1995/04/28 05:36:37;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 64.1
date: 1995/04/28 05:36:31;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 64.0
date: 1995/04/22 23:34:52;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/sr

fix dc load problem
----------------------------
revision 63.1
date: 1995/04/22 23:34:45;  author: dickson;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/clean-request,v
Working file: verilog/bsrc/sr/clean-request
head: 26.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 26.10
date: 1995/04/22 23:34:11;  author: dickson;  state: Exp;  lines: +2 -1
fix dc load problem
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr.V,v
Working file: verilog/bsrc/sr/sr.V
head: 2.32
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 32;    selected revisions: 1
description:
----------------------------
revision 2.31
date: 1995/04/22 23:34:13;  author: dickson;  state: Exp;  lines: +9 -7
fix dc load problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr.pim,v
Working file: verilog/bsrc/sr/sr.pim
head: 51.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 51.8
date: 1995/04/22 23:34:15;  author: dickson;  state: Exp;  lines: +90 -89
fix dc load problem
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr.power.tab.top,v
Working file: verilog/bsrc/sr/sr.power.tab.top
head: 39.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 39.9
date: 1995/04/28 04:51:36;  author: tbr;  state: Exp;  lines: +561 -559
update all power.tab.top files from bom 288.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/BOM,v
Working file: verilog/bsrc/tst/BOM
head: 112.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 234;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
```

```
revision 108.0
date: 1995/04/26 08:37:26;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.  Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 107.1
date: 1995/04/26 08:37:18;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 107.0
date: 1995/04/24 11:10:55;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
```

```
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 106.1
date: 1995/04/24 11:10:48;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/drvchk.V,v
Working file: verilog/bsrc/tst/drvchk.V
head: 1.85
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;    selected revisions: 1
description:
----------------------------
revision 1.81
date: 1995/04/26 08:24:15;  author: mws;  state: Exp;  lines: +16 -12
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.
============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/job.tst,v
Working file: verilog/bsrc/tst/job.tst
head: 6.41
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 41;    selected revisions: 2
description:
----------------------------
revision 6.39
date: 1995/04/26 08:24:18;  author: mws;  state: Exp;  lines: +7 -6
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
```

```
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.
----------------------------
revision 6.38
date: 1995/04/24 10:38:45;  author: mws;  state: Exp;  lines: +2 -2
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/tstrst.tst,v
Working file: verilog/bsrc/tst/tstrst.tst
head: 6.35
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 35;    selected revisions: 1
description:
----------------------------
revision 6.34
date: 1995/04/26 08:24:20;  author: mws;  state: Exp;  lines: +4 -3
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnflctI3 CJciCnflctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 8
description:
----------------------------
revision 191.0
date: 1995/04/28 05:37:13;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 190.1
date: 1995/04/28 05:37:04;  author: tbr;  state: Exp;  lines: +2 -2
```

```
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 190.0
date: 1995/04/27 00:18:06;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
iq/iq.V:  Remove dead predGoQ5 wire decl.
euterpe.status:  Over the last few BOMs:
  fullswing cb4 input to gtsnake (UUetaUTR11[2]) was fixed to halfswing,
  broken SMUX instructions were made reserved a few BOMs ago,
  ITag data out was reduced from hr to flop in choke corridor,
  ICC bus into ITag data in reg was made psuedo-diff in choke corridor.
----------------------------
revision 189.1
date: 1995/04/27 00:17:54;  author: mws;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 189.0
date: 1995/04/26 08:37:59;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

UU (and AT) placement failure is no better than before.
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
tst/drvchk.V {mg*,tst}/*?rst.tst:  Support new CEga_abm[2:0] input to LT.
tst/drvchk.V {cj,ife,tst}/*?rst.tst:  TiOrCiI3TIcnfIctI3 CJciCnfIctI3 dropped.
tst/job.tst:  Divide by 4 for missing 1:0 in AUndx1500cR12.

cp/cp.V:  Phase error made 5 tick stretcher do only 4 for lastifetch window,
  giving 20% chance of leaving icc fillotstndng on.
  Tests icacheharder2 & icache_except noticed.  Placement not affected.
euterpe.status rg/rgpc.V:  Remove obsolete concern about loading of PL to rgxmit
  and fix associated comments in rgpc.V.
euterpe.status:  Remove notes for ctioi out reg not ff & in not psuedo-diff
  which were fixed in recent BOMs.
  Add note on exception-register-lockout & CC-busy-lockout deadlock (thx woody).
  Add note on ICache fill write impairing other cylinder IFetch; limits thereof.
  Improve BGate/SynchOp illegal mem type usage comment.
----------------------------
revision 188.1
date: 1995/04/26 08:37:51;  author: mws;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 188.0
date: 1995/04/25 23:15:39;  author: woody;  state: Exp;  lines: +1 -1
```

```
Release Target: euterpe/verilog/bsrc

Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy. *not complete*

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.

placement updates to follow.
CVS: ----------------------------------------------------------------------
CVS: Enter Log.  Lines beginning with `CVS: ' are removed automatically
CVS:
CVS: Committing in
CVS:
CVS: Modified Files:
CVS:  euterpe.V
CVS: ----------------------------------------------------------------------
----------------------------
revision 187.1
date: 1995/04/25 23:15:30;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v
Working file: verilog/bsrc/uu/uu.V
head: 1.202
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 202;   selected revisions: 3
description:
issue unit
----------------------------
revision 1.183
date: 1995/04/26 23:54:01;  author: mws;  state: Exp;  lines: +8 -6
uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
```

```
----------------------------
revision 1.182
date: 1995/04/26 08:21:46;  author: mws;  state: Exp;  lines: +48 -9
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
UU placement inherited is out-of-date and now is more so.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
----------------------------
revision 1.181
date: 1995/04/25 23:07:34;  author: woody;  state: Exp;  lines: +8 -3
Partial fix for gtlbHit3C timing violation. Restructured validation of
exceptions with gtlbhit and memMgmnt.

Passed 5woody_0 and dcacheharder.

atxcenbl.pla, at.V: removed redundant reset since it is redundant. Added an
additional copy of xcenblR11 for sending to uu to validate protxcR11.

atprchk.Veqn, atpadcd.Veqn: Moved accTyp decode from atpadcd to atprchk, this
saves atoms in both places.

atprchk.Veqn, at.V: reduce loading on gtlbHit3C to try and solve timing problem.
removed gtlbHit from nbHiPri since it is a don't care since nbcin[1:0] will be
off if there is a gtlbMiss.
moved nbHiPri from atprchk to at.V to reduce size of pla and help out espresso.

at.pim: moved nbHiPri up a level of heirarchy.

euterpe.V, at, uu: ATxcenblR11 sent to uu to validate protxcr11. uu validates in
dandff.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.power.tab.top,v
Working file: verilog/bsrc/uu/uu.power.tab.top
head: 119.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 3
description:
----------------------------
revision 119.10
date: 1995/04/28 04:51:51;  author: tbr;  state: Exp;  lines: +1850 -1778
update all power.tab.top files from bom 288.0
----------------------------
revision 119.9
date: 1995/04/28 00:51:38;  author: mws;  state: Exp;  lines: +2 -2
  Make uu/UetaOutUT/u2, cp/itw05/u0, cp/itr01/u0, cp/ibw05/u0, cp/ibr01/u0
  half swing and cut power about in half, rounded up.
----------------------------
revision 119.8
```

```
date: 1995/04/26 23:54:11;  author: mws;  state: Exp;  lines: +2 -0
uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60;    selected revisions: 2
description:
----------------------------
revision 68.44
date: 1995/04/26 23:54:34;  author: mws;  state: Exp;  lines: +29 -16
uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
----------------------------
revision 68.43
date: 1995/04/26 17:23:00;  author: woody;  state: Exp;  lines: +2 -0
update placement to uu/BOM 188.0
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uumemuv.tdcd,v
Working file: verilog/bsrc/uu/uumemuv.tdcd
head: 63.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 63.13
date: 1995/04/26 08:21:51;  author: mws;  state: Exp;  lines: +106 -104
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
UU placement inherited is out-of-date and now is more so.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr7.Veqn,v
```

```
Working file: verilog/bsrc/uu/uuprblmr7.Veqn
head: 107.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 107.12
date: 1995/04/26 23:54:42;  author: mws;  state: Exp;  lines: +8 -5
uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uursrvd.tdcd,v
Working file: verilog/bsrc/uu/uursrvd.tdcd
head: 28.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 28.10
date: 1995/04/26 08:21:53;  author: mws;  state: Exp;  lines: +9 -1
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
UU placement inherited is out-of-date and now is more so.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uurst.tst,v
Working file: verilog/bsrc/uu/uurst.tst
head: 15.30
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 30;    selected revisions: 1
description:
----------------------------
revision 15.29
date: 1995/04/26 08:21:55;  author: mws;  state: Exp;  lines: +2 -2
uu/uu.V euterpe.status:  Now declare frwrd progress on an xcptn rejected by an
  already busy xcptn reg.  This prevents a deadlock of 1 cyl with xcptn reg
  and another with CC, but with 1st needing CC before bbacking.
```

```
uu/uu.V uumemuv.tdcd euterpe.V:  UU half of making bgate(i) or swapstores
  (synch ops) not to allocate-cacheable or dbuffer raise xcptn 11, illegal
  physical address.   Also extend to do same for smaller-than-octlet stores.
uu/uursrvd.tdcd:  Make SMUX reserved without disrupting other pla's.
UU placement inherited is out-of-date and now is more so.
tst/drvchk.V {cj,rg,uu}/*?rst.tst:  Support new ATprotXcEnblR11 input to UU.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uustepuu.pla,v
Working file: verilog/bsrc/uu/uustepuu.pla
head: 84.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 84.10
date: 1995/04/26 23:54:44;  author: mws;  state: Exp;  lines: +2 -2
uu/uu.V uu/uuprblmr7.Veqn uu/uu_control.pim:
  LTLB miss for trgt was accidentally getting gated off by enable for
  non-target cases.  Test ltlbga_0 noticed.
uu/uu_control.pim uu/uu.power.tab.top:
  Update for uu/BOM 188 & 189 changes (still good at 190).
uu/uustepuu.pla:  Comment that (signed) elms group does not include eulms.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/.checkoutrc,v
Working file: verilog/bsrc/xlu/.checkoutrc
head: 28.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 28.3
date: 1995/04/23 05:47:32;  author: tbr;  state: Exp;  lines: +2 -2
remove clio from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/BOM,v
Working file: verilog/bsrc/xlu/BOM
head: 65.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 6
description:
releasebom adding BOM
----------------------------
revision 60.0
date: 1995/04/28 05:37:37;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
Makefile:
      clean out chip excude list

Makefile.tst:
      uu-local-p4.pobs -> uu-local.obs

ce:
      Fix flash ce from external cerberus
      Vo fannout and timing fixes

nb:
      placement improvement

update all */*.power.tab.top files from BOM 288 top level
----------------------------
revision 59.1
date: 1995/04/28 05:37:30;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 59.0
date: 1995/04/25 06:24:53;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating the latest changes.

Top level picks up Makefile tweaks and t top level euterpe.V
chnage to match the tau gannout change in gt.

New .checkoutrc's throughout without clio:0 to satisfy the nit-hunter.

cp, ctioi new power.tab.local to fix csyn top level swing problem.
----------------------------
revision 58.1
date: 1995/04/25 06:24:42;  author: tbr;  state: Exp;  lines: +2 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 58.0
date: 1995/04/24 11:11:33;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/* at/* sr/* euterpe.V:  Other peoples' unBOMed placement/timing stuff.
ctioi/ctioi.V ctioi/ctioi.pim:  DC load violation on tau0CX[34] (sic).
  Changed the dout stage from hr to ff since we don't need hr's here anyway.
  Shortened snake read snap by 1 tick to match hr-->ff dout.

euterpe.status:  Note silly logic UUvldGoUV and clarify ITag XA field.
  Remove note that ltlb-global-access-control-per-PL upgrade needed.
  Remove note that ICache miss may restart from CC going free too soon; now that
  cc forward progress & icc fill outstanding prevent the case from happening.
ctioi/ctioi.V cp/cp.V cp/cp.pim cp/cpl.pim euterpe.V:
  Remove dies-in-ctioi CPifetchq0.
ctioi/ctioi.V ctioi/ctioi.pim ctioi/ctioi.power.tab.top \
cj/cj.V       cj/cj.pim       cj/cj.power.tab.top       euterpe.status:
  Hazard output stage was unnecessarily hr & wrong tau, resulting in missed
```

```
  collision from read 0 ticks after write.  Finally decide too confusing, so
  restructure CP and move hazard to IFe, thus changing...
ife/ife.V ife/ife.pim.txt cp/cp.V cp/cpl.pim cp/cp.power.tab.top euterpe.V
  ...as well, and un-change {cj,ctioi}/*.power.tab.top.
  This also saves random interconnect in crowded CP(lo) area (also about 100
  atoms giving room to maneuver) and speeds ICache fills about 32 ticks
  (6 major cycles) and uncached ifetch about 4 ticks (.8 major cycle).
  Also add wrtNdx[14:12] to IFe and enough compare there so that cache fills no
  longer cause mostly false collisions against IBuffer for critical other cyls.
cp/cp.V cp/cph.pim cp/cp.pim euterpe.V euterpe.status:
  Trade reset_abm for IFrstUT for release determinism & avoid need for synchro.
cp/cp.V cp/cp.pim:  Delete dead ifnc17 dorff so that Mr. Dickson can see movie.
cp/Makefile:  Pim dependency was pointing at dead cp.pim file,not new pim files.
icc/icc.V icc/icc.pim.txt euterpe.V:  Convert iGvaMiss[63:12] to
  psuedo-diff to save more than enough wires to pay for recent CP changes.
{cj,cp,ctioi,icc,ife,hz,rg,rgxmit}/.checkoutrc:
  Gards_display no longer necessary.
hz/hz.V hz/hz.pim hz/hz.power.tab.top:  Daisy chain tau should be hrbuf not ff.
  Still need ++hrbuf in GT just for GTLB (it+others too heavy for far away hz).
ife/ife.bottom.pim ife/ife.top.pim:  Recent release forgot to cvs remove these.
ife/ife_control.pim:  Recent release forgot to null this out.
rg/rg_control.pim rgxmit/rgxmit_control.pim icc/icc_control.pim:
  Mangle tool paths in comments to hide from hunt-nits.
  Also truncate & comment near-obsolete files.
tst/job.tst cj/rsrvd.tst:  Support new AUndx copy.
----------------------------
revision 57.1
date: 1995/04/24 11:11:26;  author: mws;  state: Exp;  lines: +2 -1
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/xlu.power.tab.top,v
Working file: verilog/bsrc/xlu/xlu.power.tab.top
head: 48.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 48.4
date: 1995/04/28 04:52:05;  author: tbr;  state: Exp;  lines: +740 -740
update all power.tab.top files from bom 288.0
=============================================================================
```